3V Nixie Clock

8

1800mAH

100mA ⇒ 18,000HRS
10mA ⇒ 180,000HRS

8766HR's = 1YR
1000mAH/8766 = 114μA
1000mAH/200μA = 5000HRS = 208 DAYS
7 MONTHS

1000mAH/400μA = 2500HRS (104DAYS)
@4MHZ
@1MHZ ⇒ 1000mAH/120μA → 8333HRS → 347DAYS
50WKS

BKGND
PLG
TEST
ACTV
DSPLY
EXIT
RTC
16HZ
EΦ

3V
AAAx2
Vcc
3V→1.5V
3V
1.5V
0V
1.2V

VCC
TΔΦ
2K2
10K
0.47
TΔ1
100K
0.1
47K
0.47
22K
22K
(MIN)
(HR)
VCC

Vcc
1
20
17
PB (SDA)
19
PB7 (SCK)
8
PD4
9
PD5
4
(PA1)
1.8432MHz
~1/2Yr
5
(PA0)
12
PB4
TINY 2313
PB2
14
PB3
15
PD4
16
PB6
18
PD4
2
PD1
3
PD2
6
PD3
7
MPΦ A42 x4
1K
4800HZ
PB6
11
PB1
13
10
192TICKS
470μH
1.1mA/Hr
470
1000pF
BC 639
PZTA CPC

K0
K1
K2
K3
K4
K5
K6
K7
K8
K9
A
B
C
D
470Φ
470
C
D
A
D

+60V
470K
A0
A1
A2
A3
MPΦ A42 x10
+9CV
470K
K0
K1
K5
K9
470K x14

+180V
M1
M10
H1
H10
10K
10K
10K
10K
MPΦ A42 x4
A3
A2
A1
A0
+180V
+120V
+60V
1M
1M
K0 — K9
A0 — A3
1M
2K
15K

1M
1M
1K
47pF
32KHz
5pF
47pF
120mA / 200mA
12K
47K
47pF
47pF
1K
6.8K
47K
47pF
(62CMOS)

THERMO
DZ
OCR←OCR+192
TGL
TGL/ACTV
LOW
PDG OFF
PDG ON
CNT--
EQ
CNT←4
FLAGS ACTIVE
EXIT

1 ÷ 4 8.192KHz
3 ÷ 8 4.096KHz
7 ÷ 16 2.048KHz

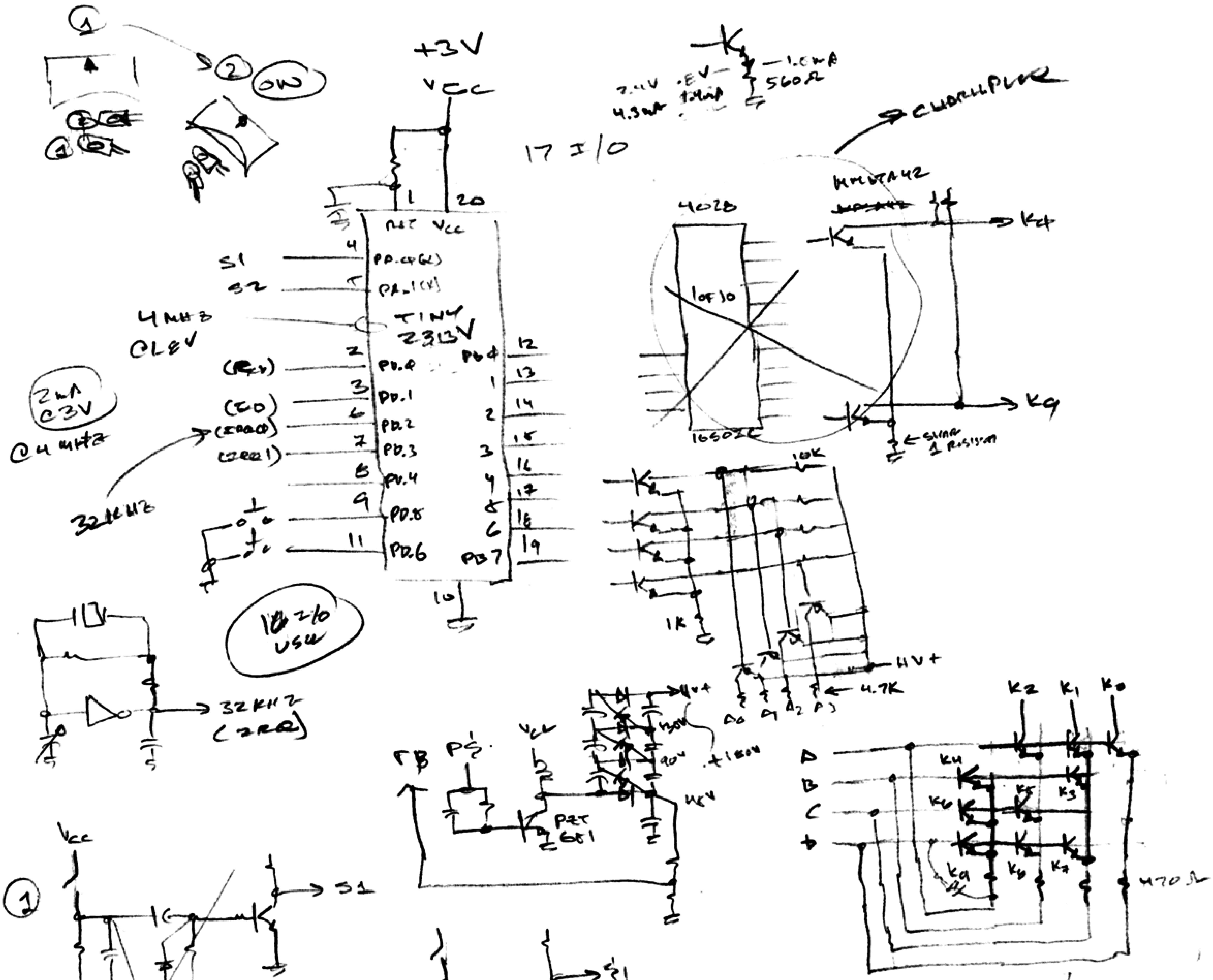
4KHz (/125)
7.8KHz/(L4)
=15625
=1SEC

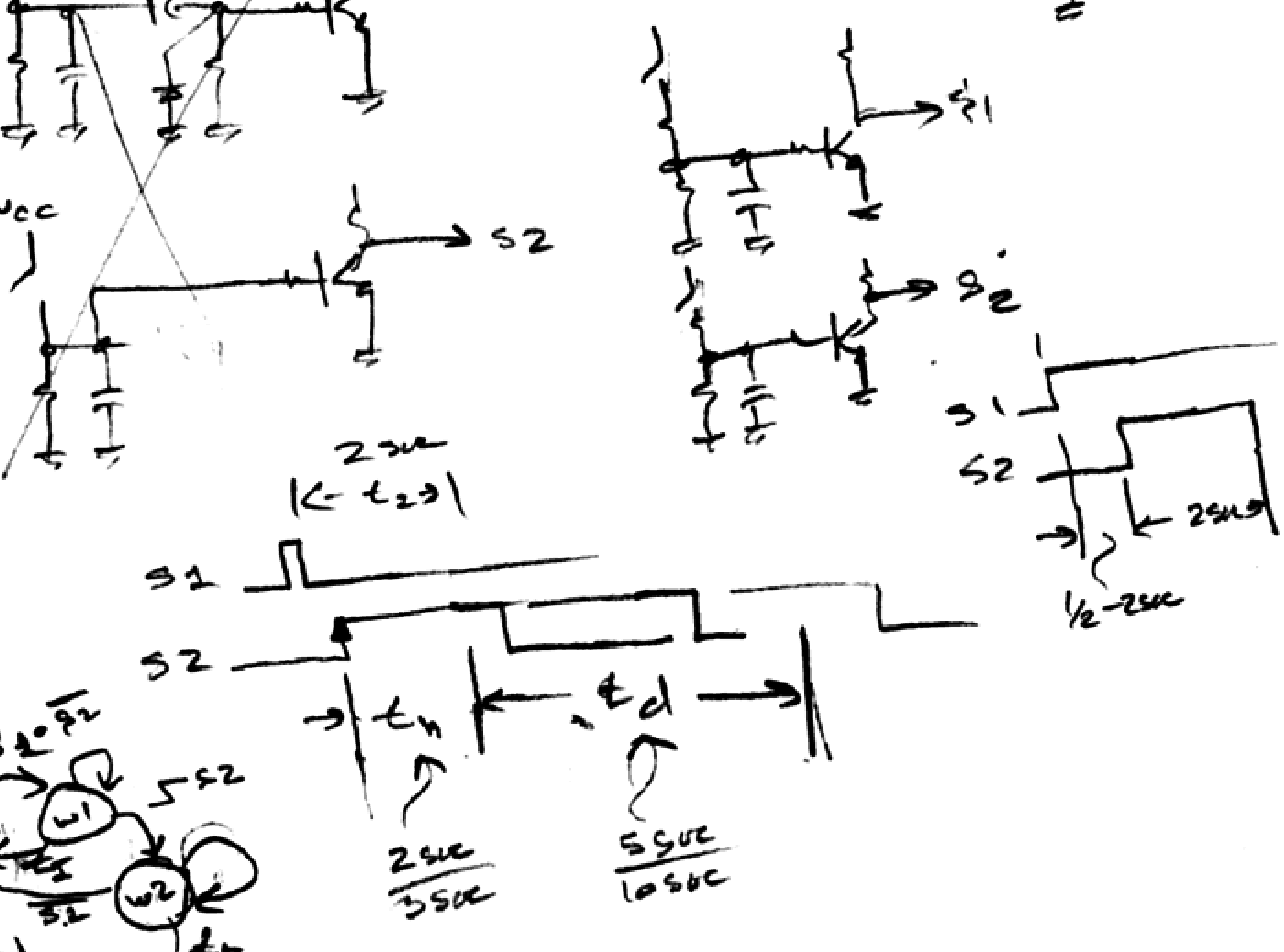
180V
100K 172V
40V
100K 60V
300mA

4096/64=64HZ
15 15 15 15 15 15 15 15
A A0 B A1 B A2 B A3 B A4
M4 M1 H1 H10
64

+120V
60V
1M
1M
2M/64=142K (422mA)

PD
7 6 5 4 3 2 1 0
— SW S1 SQ A3 A2 A1 AΦ
OUT IN IN OUT OUT OUT OUT
G 1 Φ 0 1 1 1 1 4FH



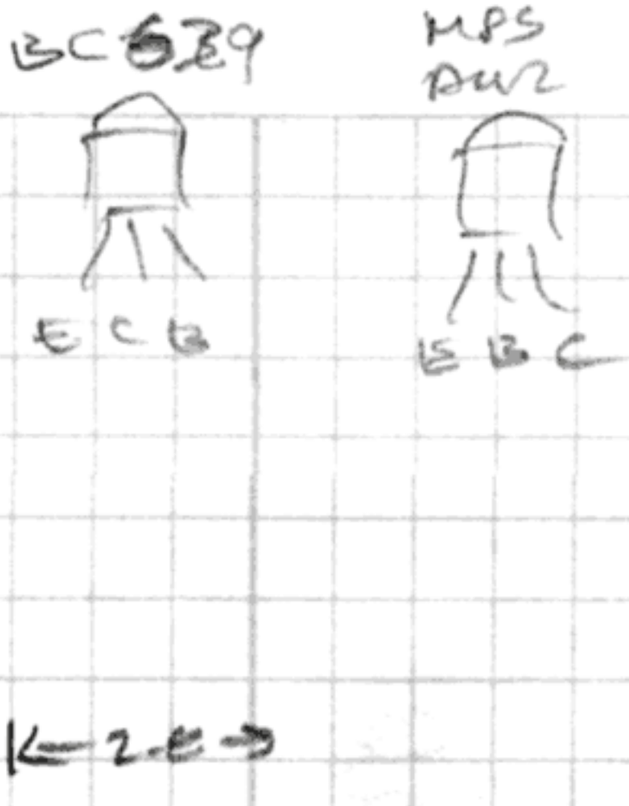


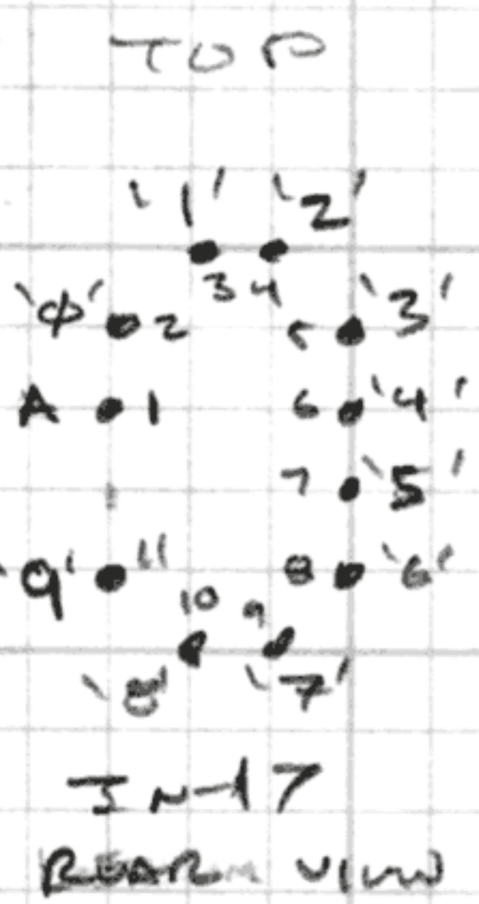
	D	C	B	A	BCD D	C	B	A
K_0	0	Z	Z	1	1	0	0	1
K_1	Z	0	Z	1	0	1	0	1
K_2	Z	Z	0	1	0	0	1	1
K_3	Z	0	1	Z	0	1	1	0
K_4	Z	Z	1	0	0	0	1	1
K_5	Z	1	0	Z	0	1	1	0
K_6	Z	1	Z	0	0	1	0	1
K_7	1	0	Z	Z	1	1	0	0
K_8	1	Z	0	Z	1	0	1	0
K_9	1	Z	Z	0	1	0	0	1
BLANK	Φ	Φ	Φ	Φ	1	1	1	1
↓	1	1	1	1	1	1	1	1

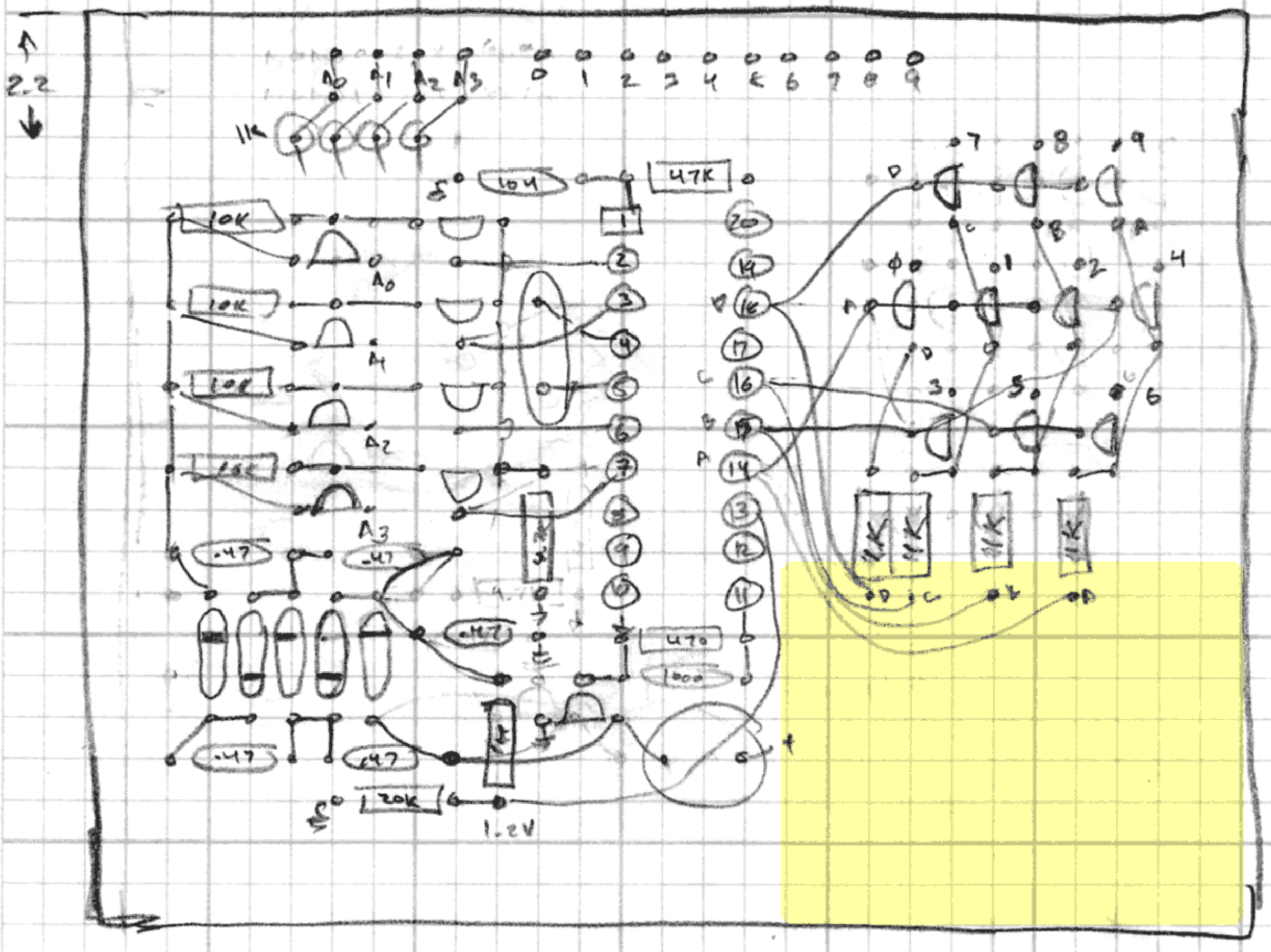
ALL BLANK INTERRUPT

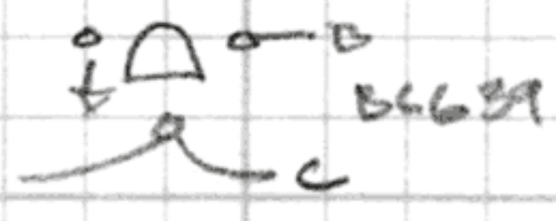
3V Nixie Clock

3V Nixie Clock





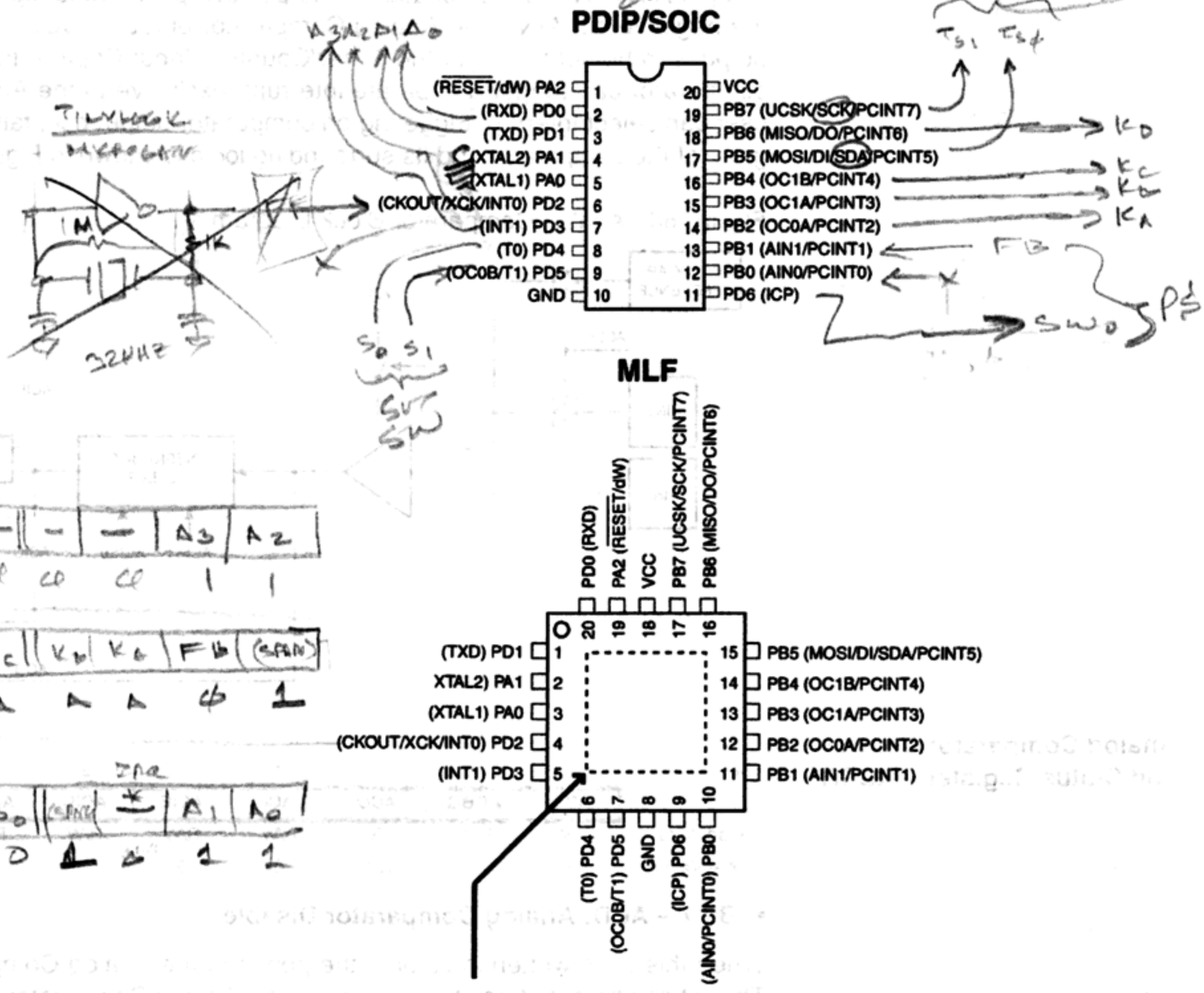




3V Nixie Clock

Pin Configurations

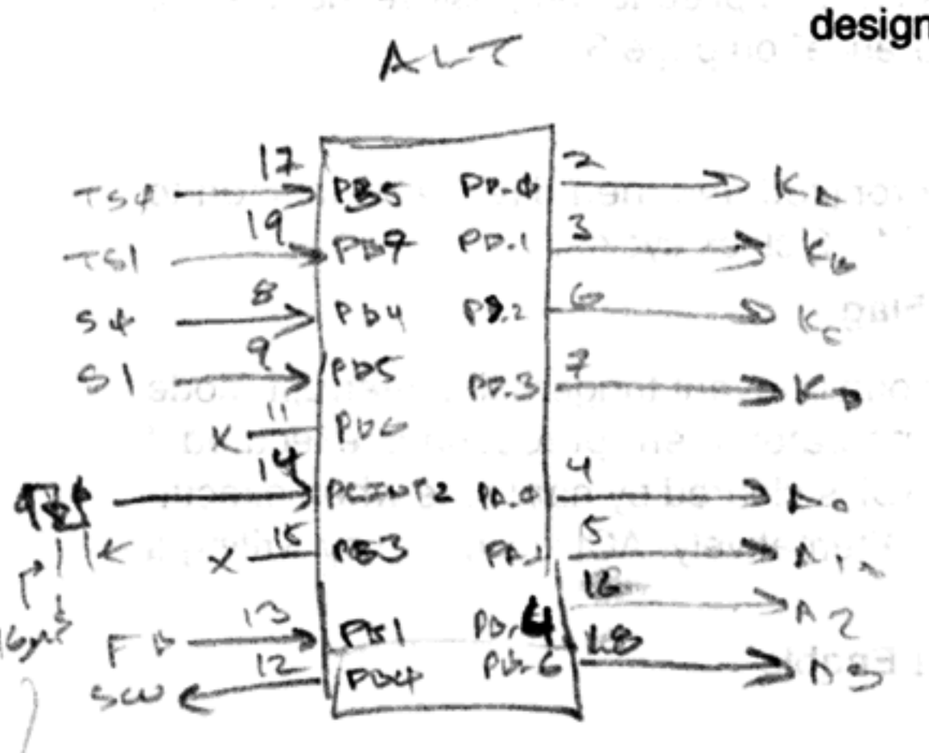
Figure 1. Pinout ATtiny2313

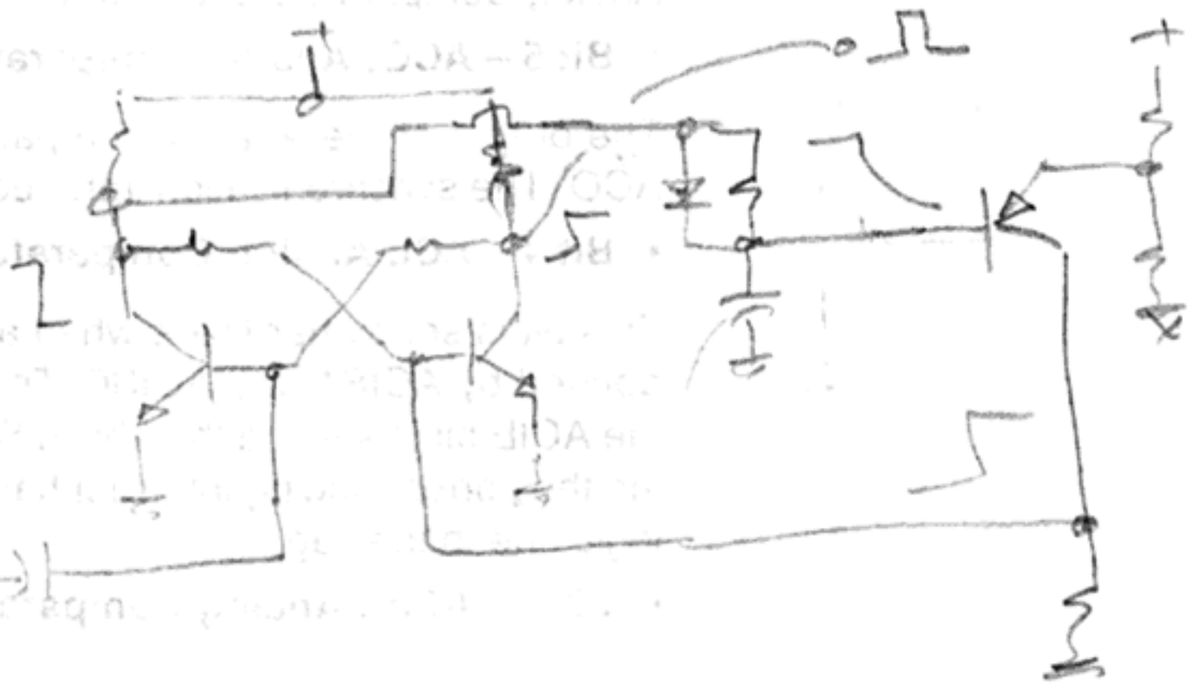


NOTE: Bottom pad should be soldered to ground.

Overview

The ATtiny2313 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny2313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

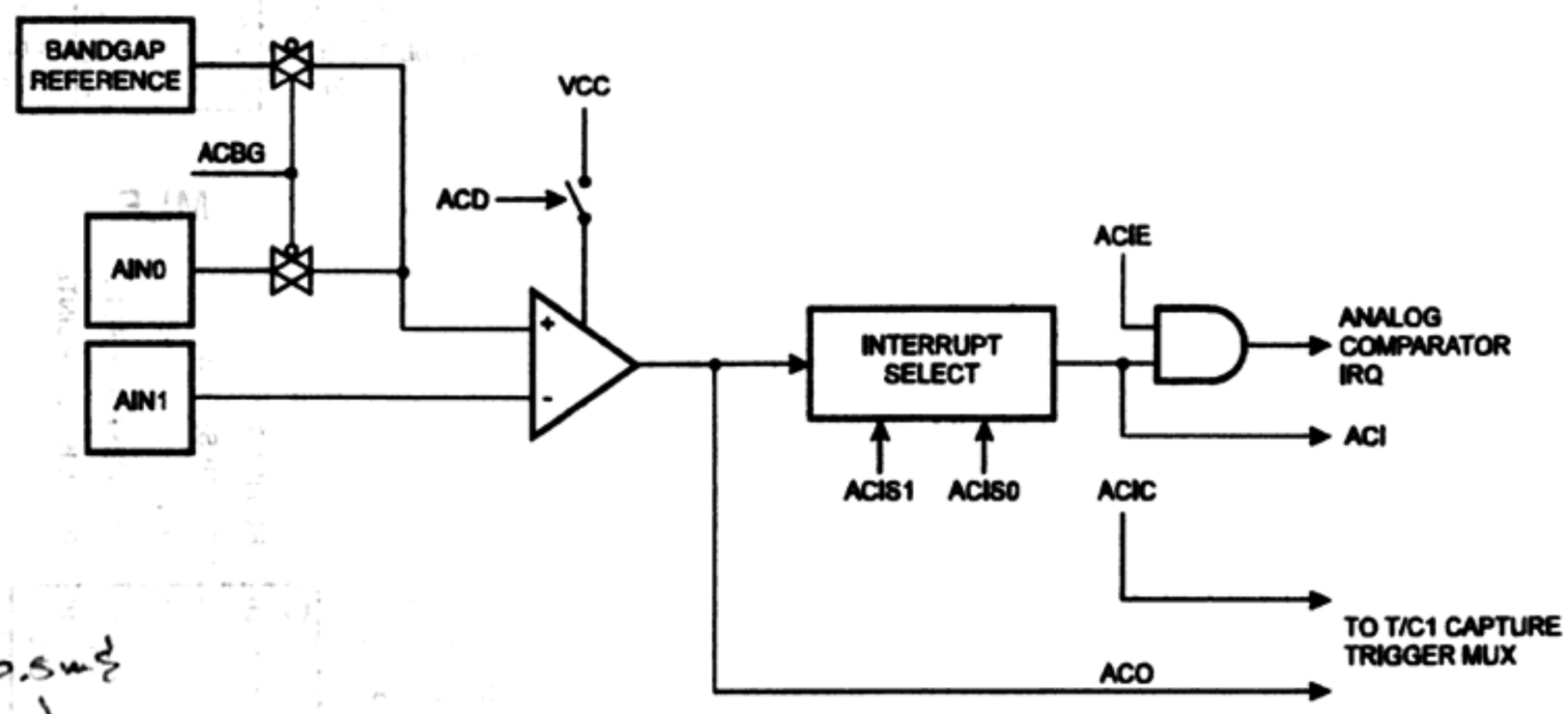




Analog Comparator

The Analog Comparator compares the input values on the positive pin AIN0 and negative pin AIN1. When the voltage on the positive pin AIN0 is higher than the voltage on the negative pin AIN1, the Analog Comparator output, ACO, is set. The comparator's output can be set to trigger the Timer/Counter1 Input Capture function. In addition, the comparator can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select Interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown in Figure 66.

Figure 66. Analog Comparator Block Diagram



Analog Comparator Control and Status Register – ACSR

Bit	7	6	5	4	3	2	1	0	
	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	ACSR
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	N/A	0	0	0	0	0	

- **Bit 7 – ACD: Analog Comparator Disable**

When this bit is written logic one, the power to the Analog Comparator is switched off. This bit can be set at any time to turn off the Analog Comparator. This will reduce power consumption in Active and Idle mode. When changing the ACD bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

- **Bit 6 – ACBG: Analog Comparator Bandgap Select**

When this bit is set, a fixed bandgap reference voltage replaces the positive input to the Analog Comparator. When this bit is cleared, AIN0 is applied to the positive input of the Analog Comparator. See "Internal Voltage Reference" on page 37.

- **Bit 5 – ACO: Analog Comparator Output**

The output of the Analog Comparator is synchronized and then directly connected to ACO. The synchronization introduces a delay of 1 - 2 clock cycles.

- **Bit 4 – ACI: Analog Comparator Interrupt Flag**

This bit is set by hardware when a comparator output event triggers the interrupt mode defined by ACIS1 and ACIS0. The Analog Comparator interrupt routine is executed if the ACIE bit is set and the I-bit in SREG is set. ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logic one to the flag.

- **Bit 3 – ACIE: Analog Comparator Interrupt Enable**

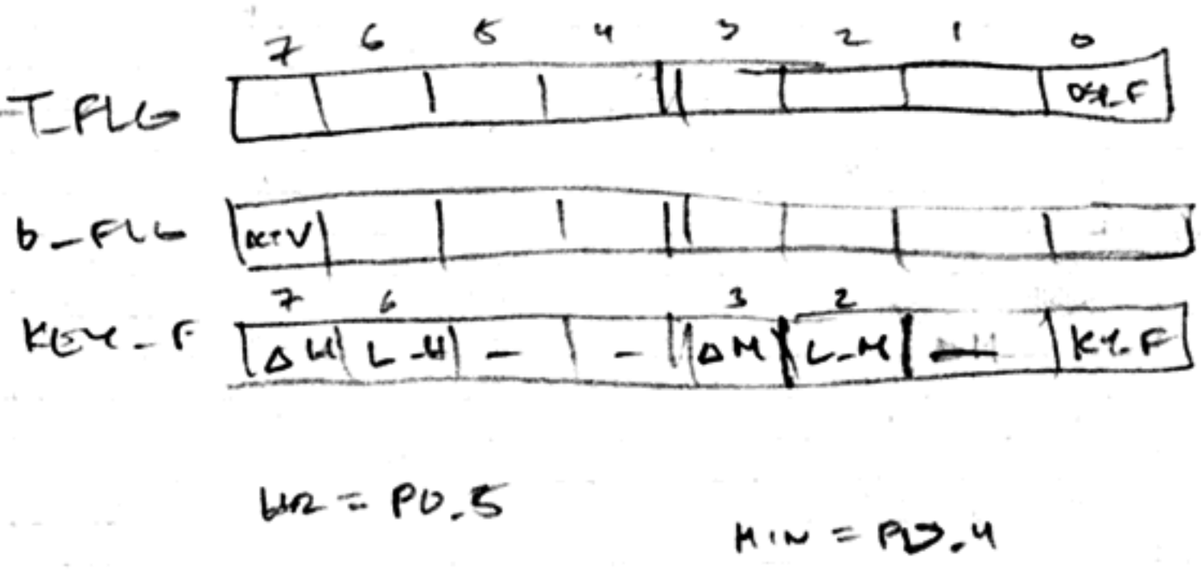
Interrupts

This section describes the specifics of the interrupt handling as performed in ATtiny2313. For a general explanation of the AVR interrupt handling, refer to "Reset and Interrupt Handling" on page 11.

Interrupt Vectors in ATtiny2313

Table 21. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	0x0000	RESET	External Pin, Power-on Reset, Brown-out Reset, and Watchdog Reset
2	0x0001	INT0	External Interrupt Request 0
3	0x0002	INT1	External Interrupt Request 1
4	0x0003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	0x0004	TIMER1 COMPA	Timer/Counter1 Compare Match A
6	0x0005	TIMER1 OVF	Timer/Counter1 Overflow
7	0x0006	TIMER0 OVF	Timer/Counter0 Overflow
8	0x0007	USART0, RX	USART0, Rx Complete
9	0x0008	USART0, UDRE	USART0 Data Register Empty
10	0x0009	USART0, TX	USART0, Tx Complete
11	0x000A	ANALOG COMP	Analog Comparator
12	0x000B	PCINT	Pin Change Interrupt
13	0x000C	TIMER1 COMPB	Timer/Counter1 Compare Match B
14	0x000D	TIMER0 COMPA	Timer/Counter0 Compare Match A
15	0x000E	TIMER0 COMPB	Timer/Counter0 Compare Match B
16	0x000F	USI START	USI Start Condition
17	0x0010	USI OVERFLOW	USI Overflow
18	0x0011	EE READY	EEPROM Ready
19	0x0012	WDT OVERFLOW	Watchdog Timer Overflow



3V Nixie Clock

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	7
0x3E (0x5E)	Reserved	–	–	–	–	–	–	–	–	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	10
0x3C (0x5C)	OCR0B	Timer/Counter0 – Compare Register B								77
0x3B (0x5B)	GIMSK	INT1	INT0	PCIE	–	–	–	–	–	59
0x3A (0x5A)	EIFR	INTF1	INTF0	PCIF	–	–	–	–	–	61
0x39 (0x59)	TIMSK	TOIE1	OCIE1A	OCIE1B	–	ICIE1	OCIE0B	TOIE0	OCIE0A	78, 109
0x38 (0x58)	TIFR	TOV1	OCF1A	OCF1B	–	ICF1	OCF0B	TOV0	OCF0A	78
0x37 (0x57)	SPMCSR	–	–	–	CTPB	RFLB	PGWRT	PGERS	SELFPRGEN	155
0x36 (0x56)	OCR0A	Timer/Counter0 – Compare Register A								77
0x35 (0x55)	MCUCR	PUD	SM1	SE	SM0	ISC11	ISC10	ISC01	ISC00	52, 59
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	36
0x33 (0x53)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	76
0x32 (0x52)	TCNT0	Timer/Counter0 (8-bit)								77
0x31 (0x51)	OSCCAL	–	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	25
0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	73
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1BO	–	–	WGM11	WGM10	104
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	*107*
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								108
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								108
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Compare Register A High Byte								108
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Compare Register A Low Byte								108
0x29 (0x49)	OCR1BH	Timer/Counter1 – Compare Register B High Byte								109
0x28 (0x48)	OCR1BL	Timer/Counter1 – Compare Register B Low Byte								109
0x27 (0x47)	Reserved	–	–	–	–	–	–	–	–	
0x26 (0x46)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	27
0x25 (0x45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								109
0x24 (0x44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								109
0x23 (0x43)	GTCCR	–	–	–	–	–	–	–	PSR10	81
0x22 (ox42)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	108
0x21 (0x41)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	41
0x20 (0x40)	PCMSK	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	61
0x1F (0x3F)	Reserved	–	–	–	–	–	–	–	–	
0x1E (0x3E)	EEAR	–	EEPROM Address Register							15
0x1D (0x3D)	EEDR	EEPROM Data Register								16
0x1C (0x3C)	EECR	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	16
0x1B (0x3B)	PORTA	–	–	–	–	–	PORTR2	PORTA1	PORTA0	57
0x1A (0x3A)	DDRA	–	–	–	–	–	DDA2	DDA1	DDA0	57
0x19 (0x39)	PINA	–	–	–	–	–	PINA2	PINA1	PINA0	57
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	57
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	57
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	57
0x15 (0x35)	GPIOR2	General Purpose I/O Register 2								20
0x14 (0x34)	GPIOR1	General Purpose I/O Register 1								20
0x13 (0x33)	GPIOR0	General Purpose I/O Register 0								20
0x12 (0x32)	PORTD	–	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	57
0x11 (0x31)	DDRD	–	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	57
0x10 (0x30)	PIND	–	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	57
0x0F (0x2F)	USIDR	USI Data Register								144
0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	145
0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	146
0x0C (0x2C)	UDR	UART Data Register (8-bit)								129
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	UPE	U2X	MPCM	129
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	131
0x09 (0x29)	UBRRL	UBRRH[7:0]								133
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	149
0x07 (0x27)	Reserved	–	–	–	–	–	–	–	–	
0x06 (0x26)	Reserved	–	–	–	–	–	–	–	–	
0x05 (0x25)	Reserved	–	–	–	–	–	–	–	–	
0x04 (0x24)	Reserved	–	–	–	–	–	–	–	–	
0x03 (0x23)	UCSRC	–	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	132
0x02 (0x22)	UBRRH	–	–	–	–	UBRRH[11:8]				133
0x01 (0x21)	DIDR	–	–	–	–	–	–	AIN1D	AIN0D	150
0x00 (0x20)	Reserved	–	–	–	–	–	–	–	–	